Honeywell

RTR-JL-03-024, Revision 0, October 01, 2003
Cage Code 09128

Single Event Effects Radiation Test Report

for the

RHrFPGA Radiation-Hardened Field-Programmable Gate Array

Honeywell Radiation Test Report #: RTR-JL-03-025

Project Number. T4516

Prepared: 01 October 2003

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Total Number of Pages: 13

Document Revision Log

Revision	Description	Date
0	Original	2003-10-01 jl/JL

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1.0 INTRODUCTION

This report describes a heavy ion single event effects (SEE) test of two RHrFPGA integrated circuits (IC). Goddard Space Flight Center (GSFC) personnel performed the test at the Texas A&M University (TAMU) cyclotron on 02 September 2003 with assistance from Honeywell's RHrFPGA design and test team.

The test characterized RHrFPGA single event upset (SEU) sensitivity to verify compliance with its soft error rate (SER) radiation design requirements. The test evaluated the FPGA using eight different test programs and FPGA configurations. Seven were optimized for SEU testing to evaluate specific internal memory elements within the FPGA, and one test program represented a current RHrFPGA application.

The RHrFPGA test devices did not experience SEU or other SEE to the maximum available test LET of 174 MeV/(mg/cm^2) at minimum rated supply voltage (3.0 volts). This result applied to all eight tests for fluences of $\geq$ 1.0x10^7 ions/cm^2 per test.

Since the devices did not upset, the test results can only establish upper bounds for SEU rates of the chip's internal storage elements. Table 1-I compares worst-case soft error rate (SER) predictions derived from the test data to the design requirements, design goals, and design analyses for the flip-flop and memory cell. Soft Error Rate includes both direct data storage SEU and captured single event transient (SET) errors that manifest themselves as an upset of the stored data. Henceforth, the term SEU will refer to either direct or SET induced upsets of the stored data. SER values in the "Step Function" column represent extreme worst-case values. Those in the "Weibull" column are also considered very conservative. The design analysis SER calculations indicate significantly lower upset rates than predictions from test results for both cell types.

Table 1-I RHrFPGA SEU Test Results, Requirements, and Design Goals.

Cell Type	Soft Error Rates (Upsets/bit/day) (1)				
	Worst-Case Predictions from Test		Criterion Values		Design Analysis (5)
	Step Function (2)	Weibull	Requirement	Design Goal	
Flip-Flop (application logic)	< 2.2x10^{-10}	< 1.3x10^{-10} (3)	< 1x10^{-7}	< 1x10^{-8}	< 5x10^{-12}
Configuration SRAM Cell	< 1.4x10^{-11}	< 3.0x10^{-16} (4)	< 1x10^{-7}	< 1x10^{-8}	< 1x10^{-18}

(1) CREME96 solar minimum galactic cosmic ray environment. No geomagnetic, 100 mil Al shielding.
(2) Assumes upset cross-section vs. LETeff curve follows a step function Weibull, see section 5.1.
(3) Assumes upset cross-section vs. LETeff curve follows a Weibull with W and S parameters equal to values determined from previous testing of similar circuits and process, see section 5.2.
(4) Assumes upset cross-section vs. LETeff curve follows a Weibull with LETo, W and S parameters equal to values determined from previous testing of 4M SRAM, see section 5.3.
(5) The design analysis calculations were provided to NASA as Critical Design Review (CDR) data for the RHrFPGA development program.

2.0 DEVICE DESCRIPTION

The RHrFPGA is an SRAM-based (soft configurable) field-programmable gate array manufactured by Honeywell using a radiation-hardened silicon on insulator fabrication process. It has 6400 user-configurable logic cells and 131,152 configuration SRAM cells. GSFC funded the development, fabrication, and radiation testing of the RHrFPGA.

3.0 TEST DESCRIPTION

The RHrFPGA heavy ion SEE test was performed at the TAMU cyclotron's SEU test facility. Ken Label of GSFC managed and operated the test. Marty Carts of Raytheon coordinated the test planning and development. Gary A. Gardner, Craig Ross, Bill Burns of Honeywell developed, supplied, and operated the characterization test set and test programs. John Lintz and Keith Golke of Honeywell provided real-time radiation test planning and data analysis support.

3.1 Test Facility and Radiation Source

Test personnel selected ions of 15 MeV/nucleon beam energy using the "in-air" irradiation station. The ion beam passes through the SEU test vacuum chamber and into open air in the SEU testing area. Before impinging on the test chip's active region the beam energy is degraded by the beam pipe exit window, an air column between the exit window and test chip, and the surface layers of the test chip. Table 3.1-I identifies the specific ion beam properties of this test. The air column was 6.0 cm for all tests, and the stopping power of the chip's surface layers is equivalent to 8.3 ?m of silicon. The degraded energy values of Table 3.1-I are calculated by TAMU. The associated LET values are from Ziegler [1] and differ by a few percent from TAMU's reported values.

Table 3.1-I Ion Beam Characteristics.

Ion	Energy (MeV)	LET (MeV/(mg/cm^2))	Angle	Degraded Energy at Die (MeV)	Effective LET at Die (MeV/(mg/cm^2))
Xe	1955	47.3	0°	1185	53.2
			60°	1076	109
Au	2955	80.2	0°	1710	85.9
			60°	1535	174

The exposure test fixture was placed on TAMU's positioning fixture, which allowed remote control of the test device position and orientation relative to the ion beam. The test fixture was oriented so angular rotation was parallel to the gate width of the test devices' transistors, thus maximizing the effective LET that could be attained. -Angular rotation was limited to $\leq$ 60° due to fixture shadowing of the die at higher incidence angles.

3.2 Test Configuration

Test personnel configured the radiation test assembly per Figure 3.2-1. An RHrFPGA test card containing two RHrFPGA devices was placed in the path of the ion beam. One RHrFPGA device was delidded and programmed to function as a test device. A second RHrFPGA device was programmed as a test controller to sequence the test and detect a SEU in the test device. It also maintained test health status and SEU error counts of the test device in a set of registers. The test controller repeatedly output the test status words to an oscilloscope that was monitored by test personnel.

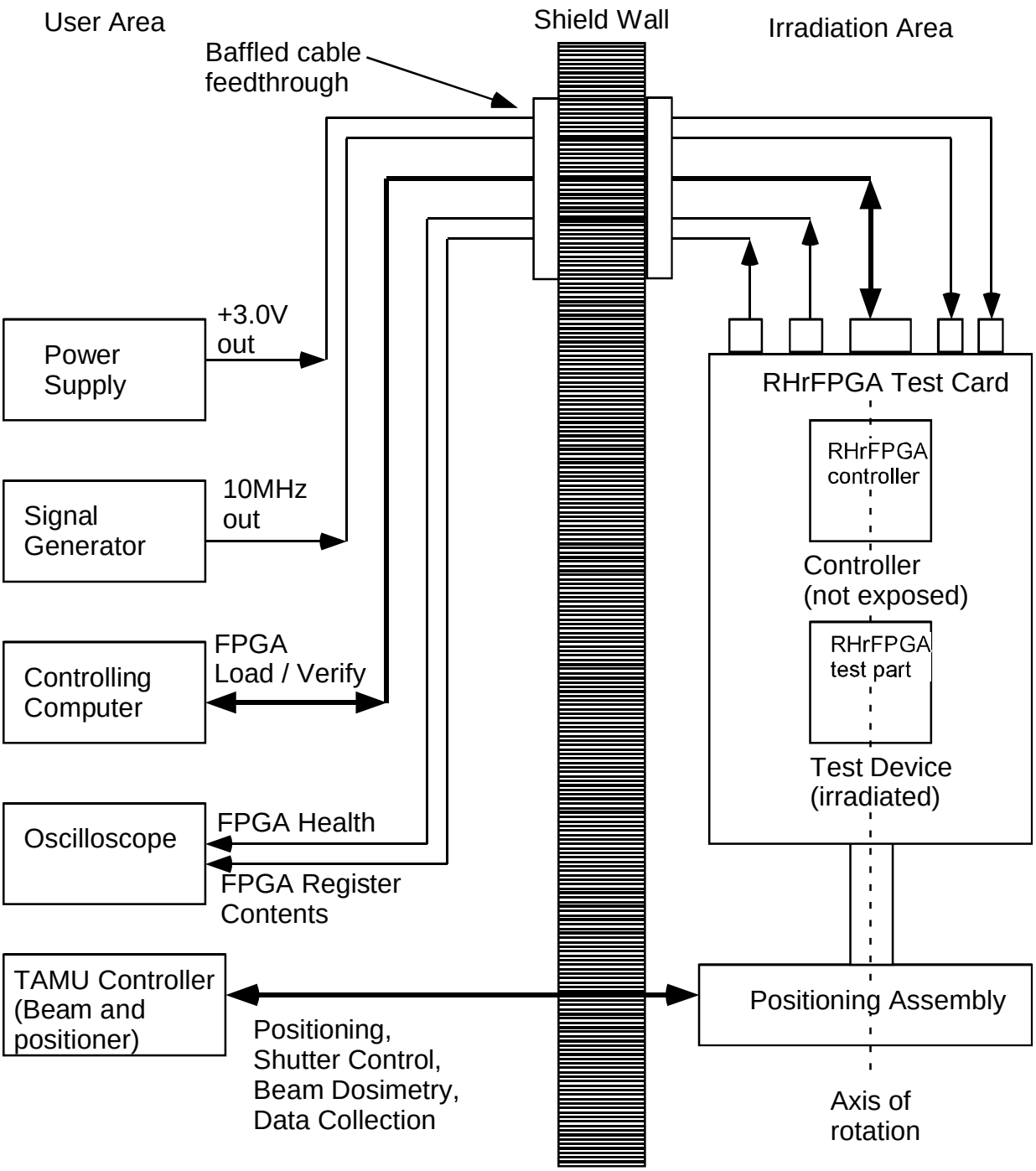

Figure 3.2-1 RHrFPGA SEU Test Assembly Configuration.

3.3 Test Programs (Vectors)

Table 3.3-I lists the eight test programs used to characterize the RHrFPGA for SEU. The “Application” test is an actual RHrFPGA application in which the RHrFPGA implements a demodulator algorithm. The “Load/Verify” tests characterize only the

configuration SRAM by monitoring it for upset during continuous configuration write and verify operations. The “Shift Register” tests the internal flip-flops by exercising multiple serial chains of shift registers. Variations of this test include specific combinatorial logic elements and interconnect logic within the chip as indicated in each test name. The associated Test Documentation package provides a more complete description of these tests and of the test circuit card functionality.

Table 3.3-I RHrFPGA Test Programs (Vectors).

Test #	Test Program Name	Abbreviated Name	Flip-Flops Tested	Config Bits Tested
1	Application with I/O (Demodulator)	Application	1506	131152
2.3	Load/Verify – Application	Load/V - App	100	131152
2.2	Load/Verify – Boot Zeros	Load/V - Boot	100	131152
3.2	Full Shift Register Vertical - Dynamic	SR-Vert-D	1450	131152
3.4	Shift Register with Logic - Dynamic	SR-Log-D	297	131152
3.5	Shift Register with Xbus - Dynamic	SR-Xbus-D	184	131152
3.6	Shift Register with Lbus - Dynamic	SR-Lbus-D	670	131152
3.7	Shift Register w/Other - Dynamic	SR-Other-D	975	131152

3.4 Test Procedure

Seventeen exposure runs were done to test the RHrFPGA for SEU and SET at VDDmin and room temperature. Two additional runs were performed at reduced VDD in order to force upsets to occur and to demonstrate that the test equipment could detect them. Test personnel followed these steps in the conduct of each exposure run. Note that the test device’s configuration SRAM was checked for upset at the conclusion of each test listed in Table 3.3-I.

1. Establish the correct test conditions (ion species, fixture position, incidence angle, supply voltage, maximum fluence setting).
2. Load the RHrFPGA controller and test device with the proper configurations to support the test. Verify that the test device and test set are functioning correctly.
3. Irradiate the test device to the desired effective fluence of $=5.0 \times 10^6$ ions/cm^2 while monitoring the device for SEU and monitoring the test set for proper health.
4. Read the controller status registers to determine the number of upsets or test anomalies that occurred in the test.
5. Read the test device configuration to check for configuration SRAM upsets.
6. Record all relevant test data from the exposure run.
7. Return to step 1 for the next exposure run until the test is finished.

4.0 TEST RESULTS

The two RHrFPGA devices did not upset to the maximum available test LET of 174 MeV/(mg/cm^2) and a maximum ion fluence of $\geq$ 1.0x10^7 ions/cm^2 or a maximum ion fluence of $\geq$ 3.5x10^{7}and 6.5x10^7 ions/cm^2 for the flip-flop and SRAM respectively if one combines the weighted fluences of shots with the same ion and angle. (The flip-flop fluences were weighted for the different numbers of sensitive flip-flops for each shot before summing). The test result was consistent with analytical predictions indicating a much higher minimum SEU LET threshold than could be attained from a heavy ion SEU test. This test consisted of 17 exposure runs at the minimum rated supply voltage of 3.0V, which is the minimum specified operating voltage and is worst-case for SEU to occur and room temperature. No other single event effects, such as SEL, were observed in this test, and no test anomalies occurred.

Test personnel performed two additional exposure runs at supply voltages below the minimum rating in an effort to verify test assembly integrity by forcing the device to upset. This is a common procedure to address the question of whether the test is actually functioning properly when upsets are not observed in the test. No upsets occurred in the first additional run (run #18) at a supply voltage of 2.1V, and two flip-flop upsets did occur in the final test run at a supply voltage of 1.8V. The configuration memory did not upset at the tested supply voltage of 2.1V or 1.8V. This exercise validated the prior test result by demonstrating the test assembly can properly detect and report upsets.

Table 4-I presents the complete RHrFPGA heavy ion SEU exposure test log.

Table 4-I RHrFPGA Single Event Effects Test Log.

Part Number:	22024887-005	Test Facility:	Texas A&M University Cyclotron SEU Test Facility
Manufacturer:	Honeywell	Ions:	Au and Xe, 15 MeV/n degraded by aramica exit window and 6.0cm air column
Description:	RHrFPGA, Digital ASIC, 0.35 micron, Custom	Test Date:	September 2, 2003
Device Serial nos:	1011-01, 1012-01 (date code 0314)	Test Personnel:	K. Label (GSFC), M. Carts (Raytheon), G. Gardner, C. Ross, B. Burns, J. Lintz
# Bits Tested:	Configuration: 131Kbits, application: ~1500 bits	Test Conditions:	10 MHz input clock, 25°C (ambient) temperature

Run #	DUT Serial #	Func-tional Test #	Test Name (Vector File)	Supply Voltage (V)	Ion Name	Angle (°)	Energy at Die* (MeV)	Effec-tive LET	Run Fluence (#/cm2)	Flux	Dose (rad(Si)	Accum Dose (rad(Si))	# Logic Upsets	# Config Upsets	Comments
1	1012-01	3.2	SR-Vert-D	3.05	Xe	0.0	1185	53.2	1.00E+07	3.3E+06	8179	8179	0	0	
2	1012-01	1.0	Application	3.05	Xe	0.0	1185	53.2	1.00E+07	3.3E+05	8179	16357	0	0	
3	1012-01	2.3	Load/V - App	3.05	Xe	0.0	1185	53.2	1.00E+07	3.4E+05	8179	24536	0	0	
4	1012-01	3.2	SR-Vert-D	3.05	Xe	60.0	1076	109.0	1.99E+07	3.3E+05	16815	41351	0	0	
5	1012-01	1.0	Application	3.05	Xe	60.0	1076	109.0	1.99E+07	3.3E+05	16815	58167	0	0	
6	1012-01	2.3	Load/V - App	3.05	Xe	60.0	1076	109.0	2.00E+07	3.3E+05	16901	75068	0	0	
7	1012-01	3.2	SR-Vert-D	3.05	Au	0.0	1710	85.9	1.00E+07	3.5E+04	13278	88346	0	0	
8	1012-01	3.2	SR-Vert-D	3.05	Au	60.0	1535	174.3	2.00E+07	3.6E+04	27192	115537	0	0	
9	1012-01	1.0	Application	3.05	Au	60.0	1535	174.3	2.00E+07	3.6E+04	27192	142729	0	0	
10	1012-01	2.3	Load/V - App	3.05	Au	60.0	1535	174.3	2.00E+07	3.5E+04	27192	169920	0	0	
11	1012-01	3.6	SR-Lbus-D	3.05	Au	60.0	1535	174.3	1.00E+07	3.7E+04	13474	183394	0	0	
12	1012-01	3.4	SR-Log-D	3.05	Au	60.0	1535	174.3	1.00E+07	3.7E+04	13474	196868	0	0	
13	1012-01	3.5	SR-Xbus-D	3.05	Au	60.0	1535	174.3	1.00E+07	3.8E+04	13474	210342	0	0	
14	1012-01	2.2	Load/V - Boot	3.05	Au	60.0	1535	174.3	1.00E+07	3.7E+04	13474	223816	0	0	
15	1011-01	3.2	SR-Vert-D	3.05	Au	60.0	1535	174.3	1.00E+07	4.2E+04	13474	13474	0	0	
16	1011-01	1.0	Application	3.05	Au	60.0	1535	174.3	1.00E+07	4.2E+04	13474	26948	0	0	
17	1011-01	2.3	Load/V - App	3.05	Au	60.0	1535	174.3	1.00E+07	4.3E+04	13474	40421	0	0	
18	1011-01	3.2	SR-Vert-D	2.1	Au	60.0	1535	174.3	1.00E+07	4.2E+04	13474	53895	0	0	Lower voltage supply to 2.1V.
19	1011-01	3.2	SR-Vert-D	1.8	Au	60.0	1535	174.3	1.00E+07	4.3E+04	13474	67369	2	0	Two flip/flop upsets at physically separate locations ~ 1/4 die apart in different scan chains.

Legend
Functional Test Number - Identifies the functional FPGA configuration tested and vector set. Corresponds to test documentation package.
Test Name - Name of test vector file used to evaluate the device under test, usually related to a specific functional block within the device.
Supply Voltage - supply voltage to the device under test, measured at the test device or test board.
Angle - Ion impingement angle on the DUT relative to the die's surface normal (a zero degree angle is perpendicular to the die surface). Rotation angles were clockwise for this test.
Energy at Die - Calculated ion energy at sensitive volume depth in the chip. Adjusted for loss in aramica window, air gap, and surface layers of chip.
Effective LET - calculated as LET at the sensitive volume depth divided by cosine of the Angle. Units are MeV-cm2/mg.
Run Fluence - exposure run ion fluence in ions/cm2. This is NOT an angle-corrected "effective fluence".
Dose - ionizing dose in silicon received during the exposure run at the sensitive volume depth.
Accum. Dose - total ionizing dose accumulated by the part under test.
logic upsets - number of single event upsets that occurred in the application during the exposure run
Config Upsets - number of single event upsets that occurred in the Configuration SRAM during the exposure run

5.0 SOFT ERROR RATE PREDICTIONS

Keith Golke of Honeywell DSES-Plymouth developed the upper bound SER predictions of Table 1-I. They are derived from the test results combined with design/layout knowledge of the RHrFPGA's internal flip-flops and memory cells, plus prior experience designing, analyzing, and SEU testing other flip-flops and memory cells..

5.1 SER calculation: step function assumption

The extreme worst-case SER (step function) values of Table 1-I are calculated based on the following assumptions for both the flip-flop and configuration SRAM cells used within the RHrFPGA.

- The SEU LETo (LET for onset of first upset) is 174 MeV/(mg/cm^2).
- The SEU cross-section steps from zero to a saturation value at LETo. The W and S Weibull parameters are set to W = 0.1 and S = 1.0 to define this step function.
- The observed saturation cross-section corresponds to sum of the gate areas of all potentially vulnerable transistors in the flip-flop or SRAM cell. However, each gate area that contributes to this observed sum is a separate sensitive volume. Since it is known which gate areas are vulnerable to a particle strike and the gate areas are known, the SER is calculated for each gate area independently. The resulting SER for each gate area are then summed for each different data storage condition.
  - The flip-flop has four data storage states:
    - Clock = High, Stored data = High
    - Clock = High, Stored data = Low
    - Clock = Low, Stored data = High
    - Clock = Low, Stored data = Low
  - The memory cell has two data storage states:
    - Stored data = High
    - Stored data = Low
- The SER for each data storage condition are averaged together to define a net SER.

5.2 SER calculation flip-flop: previous Weibull function assumption

The RHrFPGA flip-flops have some design/layout similarities to the HX3000 flip-flops. Previous SEU testing of HX3000 flip-flops resulted in LETeff versus upset cross section curves that followed the W and S Weibull parameters of W = 60 and S = 1.0. They are listed in the HX3000 Radiation Manual [2]. SERs were then calculated using the procedure described in Section 5.1 but with W = 60 and S = 1.0 instead of W =0.1 and S = 1.0.

5.3 SER calculation memory cell: 4m SRAM Weibull assumption

The configuration SRAM cell "Weibull" SER calculation assumes the SRAM cell possesses a vulnerability present in Honeywell's HX6408 4M SRAM that results in an SEU LET threshold much lower than the maximum test LET of 174 MeV/(mg/cm^2) [3]. Actually, several measures were taken in the design/layout of the RHrFPGA's configuration SRAM cell to prevent such vulnerability, and the cell design could not be made to upset in circuit simulations. Nonetheless, a SER calculation assuming the configuration SRAM cell exhibits the same values for the LETo, W and S Weibull parameters as the 4M SRAM (LETo = 3.0 MeV/mg/cm^2, W = 180 MeV/mg/cm^2, S = 1.8) but using a maximum upset cross section that fits the maximum upset cross section data at 174 MeV/mg/cm^2 from the test data results in the following:

- Maximum upset cross section based on a single shot at 174 MeV/mg/cm^2:
  Fluence = 5x10^6 ions/cm^2 for 131,152 memory cells
  Max upset cross section = 1 / (5x10^6 x 131,152) = 1.5E-12 cm^2/bit
- Fitting a Weibull with LETo = 3.0 MeV/mg/cm^2, W = 180 MeV/mg/cm^2, S = 1.8 to the above data point requires a Weibull saturated cross section of 2.6x10^{-12} ions/cm^2.

The 4M SRAM had a Weibull saturated cross section of 1.2x10^{-10} ions/cm^2. The configuration SRAM memory cell has a Weibull saturated cross section that is more than 50 times smaller which strongly suggests that the configuration SRAM memory cell does not have the same low LETo vulnerability that the 4M SRAM memory cell has.

6.0 NOTES

6.1 Acronyms

Acronym	Definition
FPGA	Field Programmable Gate Array
GSFC	Goddard Space Flight Center
IC	Integrated Circuit
LET	Linear Energy Transfer
RHrFPGA	Radiation Hardened reprogrammable Field Programmable Gate Array
SEE	Single Event Effects
SEL	Single Event Latchup
SET	Single Event Transient
SEU	Single Event Upset
SER	Soft Error Rate
SRAM	Static Random Access Memory
TAMU	Texas A&M University

6.2 References

[1] – J. F. Ziegler, *Stopping Cross-sections for Energetic Ions in All Elements,"* Vol. 5 of *"The Stopping Powers and Ranges of Ions in Matter," Pergamon Press (New York: 1977)*.
[2] – Honeywell Solid State Electronics Center, *HX3000 Radiation Manual*, p. 11, Revision 7/9/02.
[3] – S. T. Liu et al, “Single Event Effects in PDSOI 4M SRAM Fabricated in UNIBOND”, IEEE Trans. Nucl. Sci., in press, (2003).

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